## Remarks

Claims 1-37 are pending in the application and are presented for reconsideration. Claims 1, 3-9, 12-17, 19-25, 28-33, and 35-37 have been amended; claims 2, 10-11, 18, 26-27, and 34 have been canceled. No new matter has been added.

***Claim Objections***

Claims 2-16, 18, 22-23, 26, 30-31, and 34-37 are objected to for various informalities.

In particular:

Claims 2 and 18 are objected to on the grounds of insufficient antecedent basis for the limitation "said one or more chip defects". Claims 2 and 18 have been canceled, thereby rendering this object moot.

Claims 6 and 22 are objected to on the grounds of insufficient antecedent basis for the limitation "said passes simulated good". Claims 6 and 22 have been amended to correct the antecedent basis problem.

Claims 7 and 23 are objected to on the grounds of insufficient antecedent basis for the limitation "said one or more chip defects". Claims 7 and 23 have been amended to remove this limitation.

Claims 10 and 26 are objected to on the grounds of insufficient antecedent basis for the limitation "said one or more chip defects". Claims 10 and 26 have been canceled, rending this objection moot.

Claims 14 and 30 are objected to on the grounds of insufficient antecedent basis for the limitation "said passes simulated good". Claims 14 and 30 have been amended to correct the antecedent basis problem.

Claims 15 and 31 are objected to on the grounds of insufficient antecedent basis for the limitation "said one or more chip defects". Claims 15 and 31 have been amended to remove this limitation.

Claims 2-16, line 1 are objected to on the grounds that before "method" the word "A" should be changed to --The--. Claims 2-16 have been amended to overcome this objection.

Claims 34-37, line 1 are objected to on the grounds that before "integrated circuit" the word "An" should be changed to --The--. Claims 34-37 have been amended to overcome this objection.

Claims 5, 9, 25 and 29 are objected to on the grounds that the term "first" should be removed. Claims 5, 9, 25 and 29 have been amended to remove the term "first" to overcome this objection.

Applicant respectfully submits that the objections to the specification are now overcome.

***Claim Rejections***

Claims 1-2, 5-7, 10, 13-15, 17-18, 21-23, 26, 29-31, 33-34, and 36-37 are rejected under 35 U.S.C. § 102(b) as being anticipated by Erle et al. (U.S. Pat. No. 6,170,078, hereinafter "Erle").

Claims 1-37 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Erle in view of Toutounchi et al. (U.S. Pat. No. 6,594,610, hereinafter "Toutounchi").

The Examiner's rejections of the claims are respectfully traversed.

**I. Rejections of Claims Under 35 U.S.C. § 102/103**

**1. Legal standard for Rejecting Claims Under 35 U.S.C. §102/103**

Under 35 U.S.C. § 102, a claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference. *Verdegaal Bros., Inc. v. Union Oil Co.*, 814 F.2d 628 (Fed. Cir.), *cert. denied*, 484 U.S. 827 (1987).

The standard for obviousness under 35 U.S.C. §103 is whether the claimed invention would have been obvious to those skilled in the art in light of the knowledge made available by the reference or references. In re Donovan and Ryan, 184 USPQ 414, 420, n. 3 (CCPA 1975). It requires consideration of the entirety of the disclosures of the references. In re Rinehart, 189 USPQ 143, 146 (CCPA 1976). All limitations of the claims must be considered. In re Boe, 184 USPQ 38, 40 (CCPA 1974). In making a determination as to obviousness, the

references must be read without benefit of Appellants' teachings. In re Meng, 181 USPQ 94, 97 (CCPA 1974). In addition, the propriety of a 35 U.S.C. §103 rejection is to be determined by whether the reference teachings appear to be sufficient for one of ordinary skill in the relevant art having the references before him to make the proposed substitution, combination, or other modifications. In re Lintner, 173 USPQ 560, 562 (CCPA 1972).

In order to combine references, the references must suggest the combination. In re Bond, 15 USPQ2d 1566, 1568 (CAFC 1990) ('Obviousness cannot be established by combining the teachings of the prior art to produce the claimed invention, absent some teaching, suggestion or incentive supporting the combination.") (quoting Carella v. Starlight Archery and Pro Line 231 USPQ 644, 647 (CAFC 1986)). There is no suggestion to combine, however, if a reference teaches away from its combination with another source. *Tec Air Inc. v. Denso Manufacturing Michigan Inc.*, 52 USPQ2d 1294, 1298 (Fed. Cir. 1999) (*citing In re Fine* 837 F.2D 1071, 1074, 5 USPQ2d 1596, 1597 (Fed. Cir. 1988)); *See also Winner International Royalty Corp. v. Wang*, 53 USPQ2d 1580, 1587 (Fed. Cir. 2000) ("If [the cited reference] does in fact teach away from [Applicant's invention], then that finding alone can defeat [an] obviousness claim." (annotation added)). A reference may be said to teach away when a person of ordinary skill, upon reading the reference, would be discouraged from following the path set out in the reference, or would be led in a direction divergent from the path that was taken by the applicant . . . [or] if it suggests that the line of development flowing from the reference's disclosure is unlikely to be productive of the result sought by the applicant." *In re Gurley*, 27 F.3d 551, 553, 31 USPQ2d 1130, 1131 (Fed. Cir. 1994).

In addition, if when combined, the references "would produce a seemingly inoperative device," then they teach away from their combination. *Tec Air*, 52 USPQ2d at 1298 (citing *In re Sponnoble*, 405 F.2d 578, 587, 160 USPQ 237, 244 (CCPA 1969)); *See also In re Gordon*, 733 F.2d 900, 902, 221 USPQ 1125, 1127 (Fed. Cir. 1984) (finding no suggestion to modify a prior art device where the modification would render the device inoperable for its intended purpose).

The suggestion to combine references must have been in the prior art at the time Applicant's invention was made. W. L. Gore & Associates, Inc. v. Garlock, Inc., 220 USPQ 303, 312 (CAFC 1983), cert. denied, 469 U.S. 851 (1984). The mere absence from a reference of an explicit requirement of the claim cannot reasonably construed as an affirmative statement that the requirement is in the reference. *In re Evanega*, 829 F.2d 1110, 4 USPQ2d 1249 (Fed. Cir. 1987).

"The decisionmaker must view the prior art without reading into that art appellant's teachings. The issue, then, is whether the teachings of the prior art would, *in and of themselves and without the benefits of appellant's disclosure,* make the invention as a whole, obvious." In re Nomiya, Kohisa, and Matsumura, 184 USPQ 607 ,612 (CCPA 1975) (citations omitted) (quoting In re Sponnoble, 160 USPQ 237, 243 (CCPA 1969)).

**2. Response to Rejections of Claims Under 35 U.S.C. § 102**

***a. Claims 1-9 and 12-16***

Applicant's amended claim 1 recites:

> A method for verifying an integrated circuit device test for testing an integrated circuit device, said method comprising the steps of:
> simulating a flawed integrated circuit device design comprising a good integrated circuit design modified to include one or more known physical flaws in the good integrated circuit device design;
> simulating said integrated circuit device test to test said simulated flawed integrated circuit device design; and
> determining whether said simulated test of said simulated flawed integrated circuit device design discovered said one or more known physical flaws in said simulated flawed integrated circuit device design.

***The Erle Reference***

The Examiner cites Erle as anticipating claim 1. In particular, the Examiner states that Erle discloses a method (col. 1, lines 5-10) for verifying an integrated circuit device test for testing an integrated circuit device, said method comprising the steps of: simulating a flawed integrated circuit device (faulty device behavior model) comprising one or more known flaws (predetermined faulty behavior) in an integrated circuit device design (col. 1, lines 55-59 and col.

2, lines 60-63); simulating a test of said simulated flawed integrated circuit device (col. 1, lines 48-54 and col. 2. lines 63-65); and determining whether said simulated test of said simulated flawed integrated circuit device discovered said one or more known flaws in said flawed integrated circuit device (col. 1, lines 65-67; col. 2, lines 1-4 and 65-67, and col. 3, lines 1-6).

Applicant's Claim 1 is directed at verifying that an integrated circuit device test will discover certain known "defects" rather than merely modeled "faults". As described in the background section of Applicant's specification, "a 'defect' is a *physical flaw* on the integrated circuit that may be the result of poor design (e.g., missing links), poor fabrication (e.g., malformed vias or solder connections), or external events (e.g., particle contamination, change in environment such as a change in temperature that destroys all or a portion of the device). A 'fault' is a model of a problem (e.g., a bit is stuck in a high or low state, or the operating current of the device is above a pre-defined threshold). For example, a stuck-at 'fault' may indicate that a link of a transistor is broken, whereas the "defect" that caused the fault may be that the metal lines that fabricate the transistor were laid down incorrectly." (Applicant's Specification, page 4, lines 14-23).

As further described in Applicant's specification, "test development tends to be focused on detecting identifiable faults and passing good parts if they do not exhibit the faults. ....[B]ecause the test development process favors fault modeling (or detection of *symptoms* of defects rather than the defect itself), the test may actually miss detection of the defect itself, and falsely pass a defective part. What is needed, therefore, is a technique for verifying that that a test fails parts with actual defects rather than merely detecting the symptoms of defects through fault detection. Accordingly, the invention allows simulation of the integrated circuit device as if it had known defects, rather than merely fault modeling the device, and verifies that the test actually catches the defects". (Applicant's Specification, page 4, line 24 through page 5, line 9).

Applicant's Claim 1 has been amended to recite "simulating a flawed integrated circuit device design comprising a good integrated circuit design modified to include one or more known *physical* flaws in the good integrated

circuit device design". As described previously, a defect is a physical flaw, whereas a fault is a behavioral model of a problem, which may include a particular symptom of a particular type of defect. Erle does not teach or suggest "simulating a flawed integrated circuit device design comprising a good integrated circuit design modified to include one or more known *physical* flaws in the good integrated circuit device design". Erle utilizes faulty behavioral models 106 to 108 that are functional representations of devices having predetermined "defects". Please note that Erle utilizes the term "defect" not to mean a "physical flaw" as in Applicant's Claim 1, but to mean what Applicant terms a "fault". This is evidenced by the fact that all of the behavior models taught or suggested by Erle are what Applicant terms a "fault" - that is, Erle discloses only behavior models including a stuck-at-0 fault model, a stuck-at-1 fault model, a Short or Bridging Fault Model, or an Open Fault Model. For example, in Erle, a stuck-at-0 defect is defined as maintaining a particular bit at a zero value regardless of what value is being written to or read from the bit. (Erle, col. 1, lines 61-63). Clearly, this is not a physical flaw (such as a ) but is a behavior problem or symptom (what Applicant terms a "fault").

Erle is merely an example of prior art testing techniques that model faults - that is, Earl's system detects a *symptom* (i.e., a stuck bit) of a defect rather than detecting the presence of the defect (i.e., *physical* flaw) itself. Erle's technique does not verify that the test will actually discover a defect in a device under test - it merely checks to see if the test will discover a particular fault (or symptom of a defect), in this case a stuck bit. However, as pointed out in the background section of Applicant' specification, a defect may not necessarily result in the particular fault being tested for (in Erle's illustrative example, a stuck bit). Thus, using Erle's technique such a defect may go undetected by the test, thereby allowing a defective part to pass. This is a classic example of the test development approach that heavily favors not failing good parts (Applicant's Specification, page 4, lines 29-32) while overlooking verification that the test does not pass bad parts (Applicant's Specification, page 4, lines 32-34). In

summary, Erle discloses only fault modeling and does not teach or suggest simulating an integrated circuit device having a *physical* flaw.

Erle also does not teach or suggest "simulating said integrated circuit device test to test said simulated flawed integrated circuit device design" as recited in Applicant's Claim 1. As described above, Applicant's "flawed integrated circuit device" includes a *physical* flaw. Erle does not simulate the physical flaw but merely models a fault (which may or may not show up as a possible symptom of a physical flaw). Thus, Erle's system simulates a faulty behavior model and not a "flawed integrated circuit device" as required by Applicant's Claim 1.

Erle also does not teach or suggest "determining whether said simulated test of said simulated flawed integrated circuit device design discovered said one or more known physical flaws in said simulated flawed integrated circuit device design" as recited in Applicant's Claim 1. Erle teaches only comparing the outputs of a good device 104 to each of the faulty devices 106-108 to determine if the test pattern detected differences therebetween. However, such a comparison is only indicative of whether the applied test pattern detects differences between good integrated circuit devices and integrated circuit devices that exhibit the particular fault. The comparison is not indicative of whether the applied test pattern detects differences between good integrated circuit devices and integrated circuit devices that contain a physical flaw because the physical flaw itself is not modeled in Erle's behavior models. Accordingly, Erle does not meet the limitation "determining whether said simulated test of said simulated flawed integrated circuit device design discovered said one or more known physical flaws in said simulated flawed integrated circuit device design".

Since Erle does not meet each and every limitation of Applicant's claim 1, per *Verdegaal Bros., Inc., supra*, Erle cannot be used in formulating an anticipation rejection under 35 U.S.C. § 102.

***The Toutounchi Reference***

The Examiner cites Toutounchi as disclosing generating said integrated circuit device design that meets specifications of said integrated circuit device

(fig. 2, step 122, col. 3, lines 49-62), verifying that said test passes simulated good integrated circuit devices of said generated integrated circuit device design (fig. 2, step 124, col. 3, lines 63-65), indicating that said test of said simulated flawed integrated circuit device is flawed if said simulated test of said simulated flawed integrated circuit device does not discover one or more of said known flaws in said flawed integrated circuit device (col. 3, lines 65-67, col. 4, lines 1-35).

However, Toutounchi does not make up for the deficiencies of Erle in meeting Applicant's Claim 1. First, Toutounchi does not teach or suggest "a flawed integrated circuit device design comprising *a good integrated circuit design modified to include one or more known physical flaws* in the good integrated circuit device design" as recited in Applicant's Claim 1 and as missing from the Erle reference. Toutounchi teaches utilizing programmable logic devices (such as FPGAs) to emulate faults instead of modifying a good integrated circuit design to include physical flaws and then simulating the flawed integrated circuit design. (Toutounchi, col. 3, lines 14-16). In Toutounchi, no good integrated circuit design is modified. Furthermore, Toutounchi does not *simulate* anything; rather Toutounchi only emulates flaws using an FPGA. Still further, Toutounchi does not even emulate a "*physical* flaw". Toutounchi merely models a fault, such as open/short faults. Toutounchi does not model a physical flaw such as a malformed via or solder connection, or particle contamination of a section of the integrated circuit device. Toutounchi only models the behavior of the device, e.g., an open or short, but not an underlying physical flaw that may be cause of such symptom. Thus, since Toutounchi neither "simulates" nor simulates "simulating a flawed integrated circuit device design comprising a good integrated circuit design modified to include one or more known *physical* flaws in the good integrated circuit device design", Toutounchi does not meet the limitation "simulating a flawed integrated circuit device design comprising a good integrated circuit design modified to include one or more known physical flaws in the good integrated circuit device design" as recited in Applicant's Claim 1.

Toutounchi also does not teach or suggest "simulating said integrated circuit device test to test said simulated flawed integrated circuit device design" as recited in Applicant's Claim 1. As described above, Toutounchi teaches neither "simulating" nor "a flawed integrated circuit device comprising one or more known *physical flaws*". Thus, Toutounchi does not meet this limitation.

Toutounchi also does not teach or suggest "determining whether said simulated test of said simulated flawed integrated circuit device design discovered said one or more known physical flaws in said simulated flawed integrated circuit device design" as recited in Applicant's Claim 1. Again, Toutounchi teaches neither "simulating" nor "a flawed integrated circuit device comprising one or more known *physical flaws*".

Since Toutounchi does not make up for the deficiencies of Erle in meeting the limitations of Applicant's Claim 1, Erle cannot even be combined with Toutounchi to formulate an obviousness-type rejection under 35 U.S.C. § 103.

Accordingly, Applicant respectfully submits that the 35 U.S.C. § 102 and § 103 rejections of Claim 1 should be withdrawn and that Claim 1 is now in position for allowance.

Claims 3-9 and 12-16 each depend from independent base Claim 1 and add further limitations. For at least the same reasons that Claim 1 is not shown, taught, or disclosed by the cited references, Claims 3-9 and 12-16 are likewise not shown, taught, or disclosed. Thus, Applicant respectfully submits that the rejection of Claims 3-9 and 12-16 should be withdrawn.

***b. Claims 17, 19-25 and 28-32***

Claim 17 recites similar limitations to Claim 1, including the identical limitations "simulating a flawed integrated circuit device design comprising one or more known physical flaws in a good integrated circuit device design", "simulating said integrated circuit device test to test said simulated flawed integrated circuit device", and "determining whether said simulated test of said simulated flawed integrated circuit device discovered said one or more known physical flaws in said simulated flawed integrated circuit device". For at least the same reasons that Claim 1 is not shown, taught, or disclosed by the cited

references, Claim 17 is likewise not shown, taught, or disclosed. Thus, Applicant respectfully submits that the rejection of Claim 17 should be withdrawn.

Claims 19-25 and 28-32 each depend from independent base claim 17 and add further limitations. For at least the same reasons that Claim 17 is not shown, taught, or disclosed by the cited references, Claims 19-25 and 28-32 are likewise not shown, taught, or disclosed. Thus, Applicant respectfully submits that the rejection of claims 19-25 and 28-32 should be withdrawn.

***c. Claims 33 and 35-37***

Claim 33 now recites:

> An integrated circuit device test verification apparatus, comprising:
> an integrated circuit device simulator which simulates a flawed integrated circuit device design, said flawed integrated circuit device design comprising a good integrated circuit design modified to include one or more known physical flaws in the good integrated circuit device design;
> a tester simulator which simulates an integrated circuit device test executing on an integrated circuit device tester that generates test stimuli, applies said generated test stimuli to said simulated flawed integrated circuit device design, and receives test responses from said simulated flawed integrated circuit device design; and
> a simulated test results analyzer which determines whether said simulated integrated circuit device test of said simulated flawed integrated circuit device design discovered said one or more known physical flaws in said flawed integrated circuit device design.

Claim 33 recites similar limitations to Claim 1, including "an integrated circuit device simulator which simulates a flawed integrated circuit device design, said flawed integrated circuit device design comprising a good integrated circuit design modified to include one or more known physical flaws in the good integrated circuit device design", "a tester simulator which simulates an integrated circuit device test executing on an integrated circuit device tester that generates test stimuli, applies said generated test stimuli to said simulated flawed integrated circuit device design, and receives test responses from said simulated flawed integrated circuit device design", and "a simulated test results analyzer which determines whether said simulated integrated circuit device test of said simulated flawed integrated circuit device design discovered said one or more known physical flaws in said flawed integrated circuit device design". For

at least the same reasons that Claim 1 is not shown, taught, or disclosed by the cited references, Claim 33 is likewise not shown, taught, or disclosed. Thus, Applicant respectfully submits that the rejection of Claim 33 should be withdrawn.

Claims 35-37 each depend from independent base claim 33 and add further limitations. For at least the same reasons that Claim 33 is not shown, taught, or disclosed by the cited references, Claims 35-37 are likewise not shown, taught, or disclosed. Thus, Applicant respectfully submits that the rejection of claims 35-37 should be withdrawn.

## Conclusion

In view of the foregoing remarks, it is respectfully submitted that none of the references cited by the Examiner taken alone or in any combination shows, teaches, or discloses the claimed invention, and that Claims 1, 2-9, 12-17, 19-25, 28-33 and 35-37 are in condition for allowance. Reexamination and reconsideration are respectfully requested.

Should the Examiner have any questions regarding this amendment, or should the Examiner believe that it would further prosecution of this application, the Examiner is invited to call the undersigned.

Respectfully submitted,

July 6, 2006

Jessica Costa

Jessica Costa, Reg. No. 41,065

The Law Offices of Jessica Costa, PC
P.O. Box 460 Crozet, VA
22932-0460
(434) 823-2232
(434) 823-2242 (fax)